

## 20A, 600V N-CHANNEL MOSFET

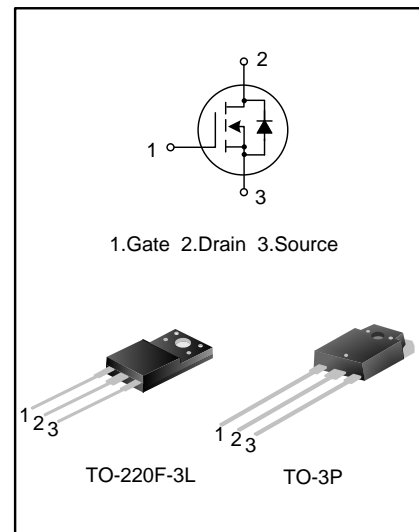
### GENERAL DESCRIPTION

SVF20N60F/PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

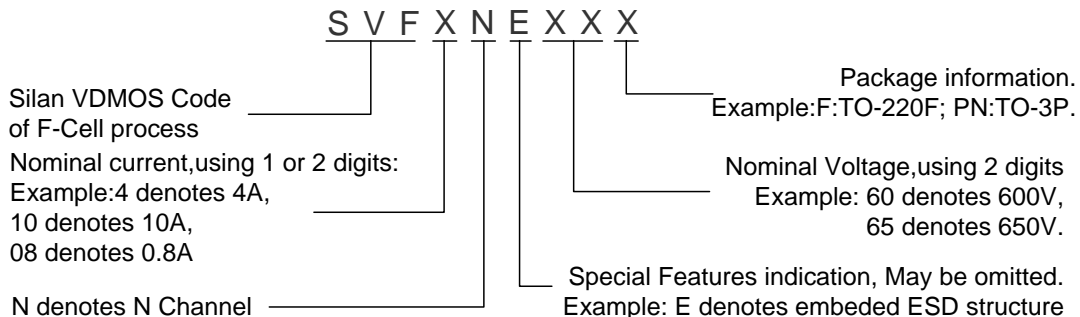
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

### FEATURES

- ◆ 20A,600V, $R_{DS(on)(typ.)}=0.28\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



### NOMENCLATURE



### ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF20N60F	TO-220F-3L	SVF20N60F	Pb free	Tube
SVF20N60PN	TO-3P	20N60	Pb free	Tube

**ABSOLUTE MAXIMUM RATINGS (T<sub>c</sub>=25°C unless otherwise noted)**

Characteristics	Symbol	Ratings		Unit
		SVF20N60F	SVF20N60PN	
Drain-Source Voltage	V <sub>DS</sub>	600		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current	I <sub>D</sub>	20.0		A
		12.6		
Drain Current Pulsed	I <sub>DM</sub>	80.0		A
Power Dissipation(T <sub>c</sub> =25°C) -Derate above 25°C	P <sub>D</sub>	74	258	W
		0.59	2.06	W/°C
Single Pulsed Avalanche Energy(Note 1)	E <sub>AS</sub>	1433		mJ
Operation Junction Temperature Range	T <sub>J</sub>	-55~+150		°C
Storage Temperature Range	T <sub>stg</sub>	-55~+150		°C

**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Ratings		Unit
		SVF20N60F	SVF20N60PN	
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.69	0.48	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	50	°C/W

**ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B <sub>VDS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	600	--	--	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V	--	--	1.0	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	--	--	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10.0A	--	0.28	0.35	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz	--	2708	--	pF
Output Capacitance	C <sub>oss</sub>		--	293	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	6.6	--	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =300V, I <sub>D</sub> =20.0A, R <sub>G</sub> =25Ω, (Note2,3)	--	27.0	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	44.0	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	82.0	--	
Turn-off Fall Time	t <sub>f</sub>		--	44.4	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =480V, I <sub>D</sub> =20.0A, V <sub>GS</sub> =10V, (Note 2,3)	--	47.45	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	14.13	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	14.51	--	

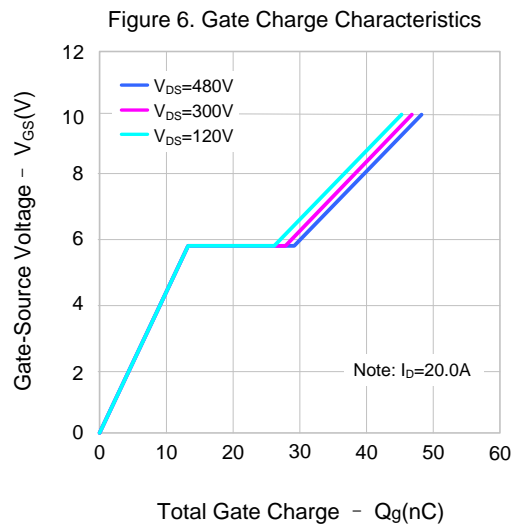
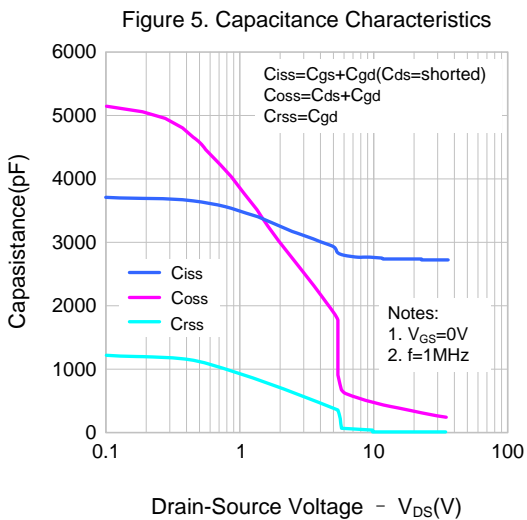
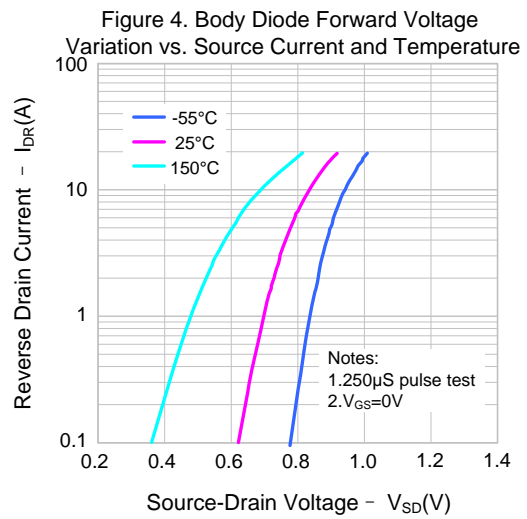
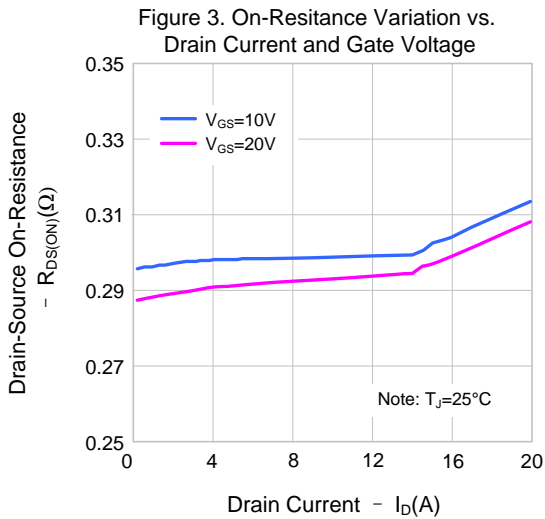
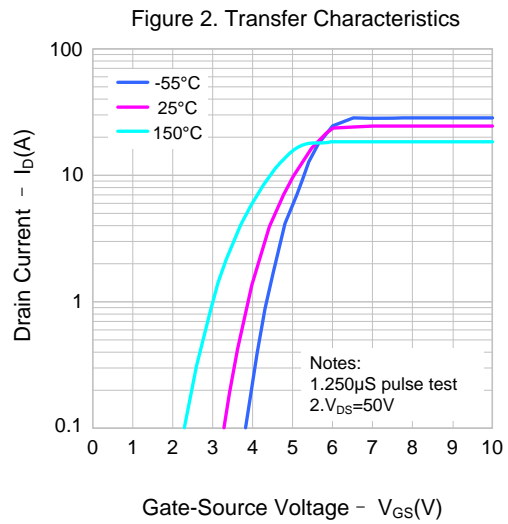
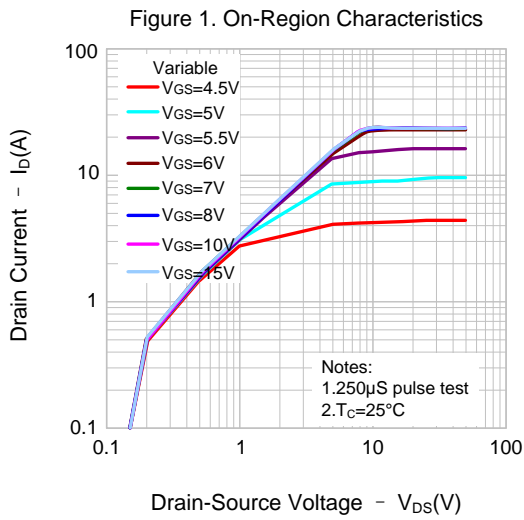
## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction	--	--	20.0	A
Pulsed Source Current	$I_{SM}$	Diode in the MOSFET	--	--	80.0	
Diode Forward Voltage	$V_{SD}$	$I_S=20.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	$T_{rr}$	$I_S=20.0A, V_{GS}=0V,$	--	630.1	--	ns
Reverse Recovery Charge	$Q_{rr}$	$di_F/dt=100A/\mu s$ (Note 2)	--	8.19	--	$\mu C$

### Notes:

1.  $L=30mH, I_{AS}=9.45A, V_{DD}=100V, R_G=25\Omega,$  starting  $T_J=25^\circ C$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s,$  Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**



**TYPICAL CHARACTERISTICS(continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

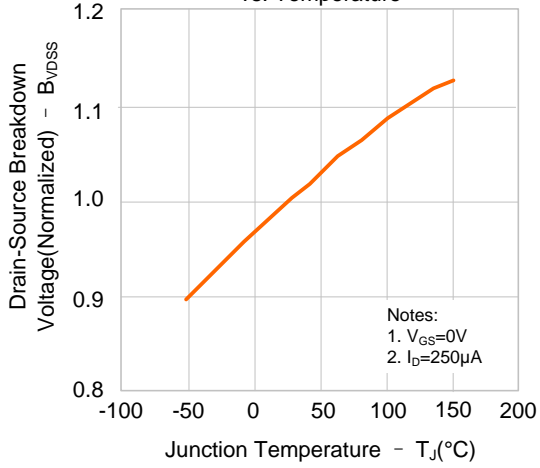


Figure 8. On-resistance Variation vs. Temperature

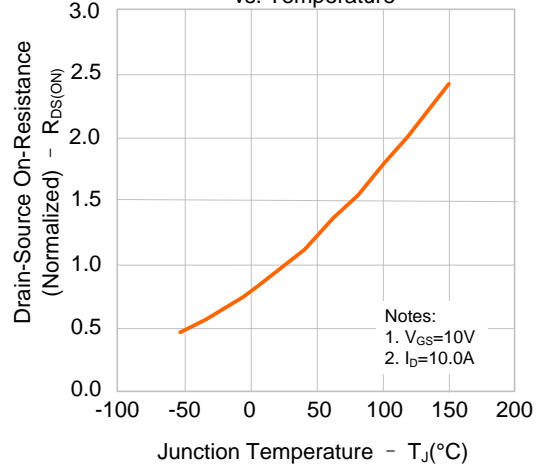


Figure 9-1. Max. Safe Operating Area(SVF20N60F)

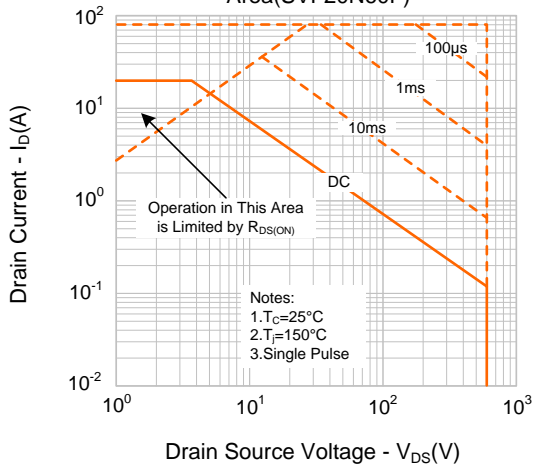


Figure 9-2. Max. Safe Operating Area(SVF20N60PN)

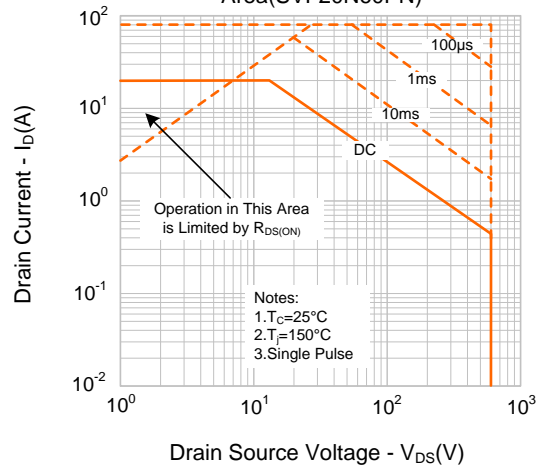
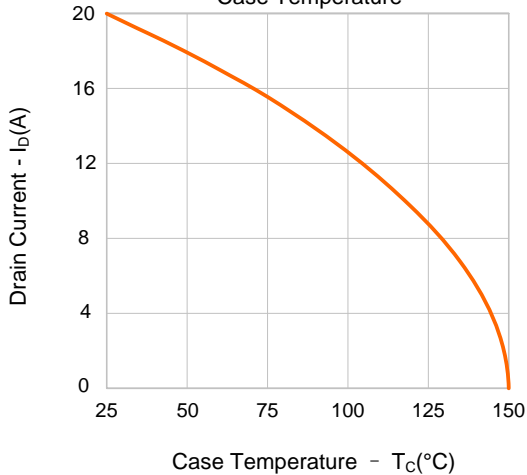
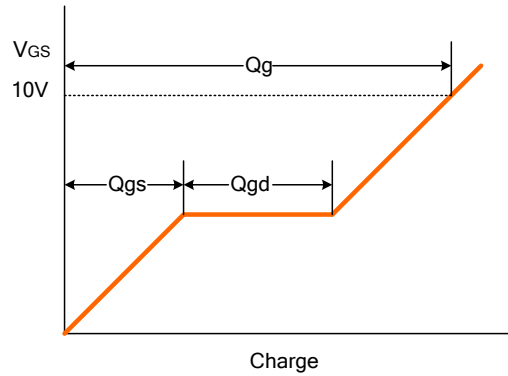
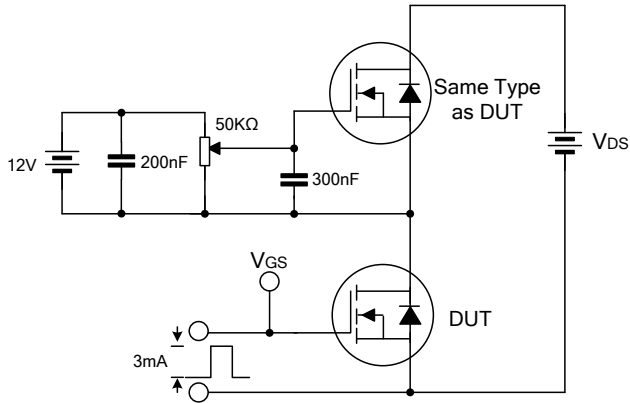


Figure 10. Maximum Drain Current vs. Case Temperature

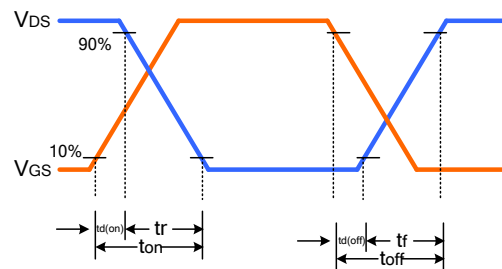
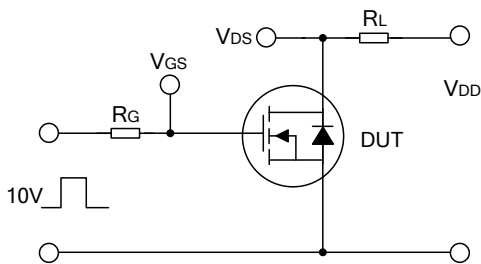


**TYPICAL TEST CIRCUIT**

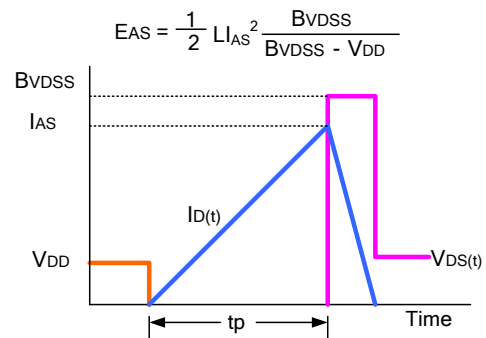
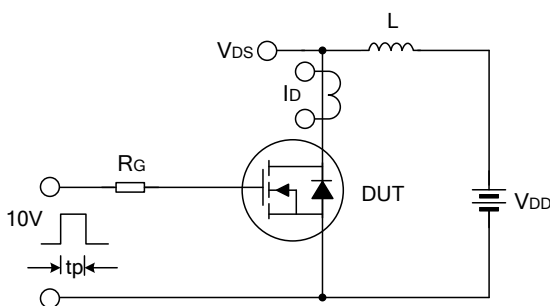
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



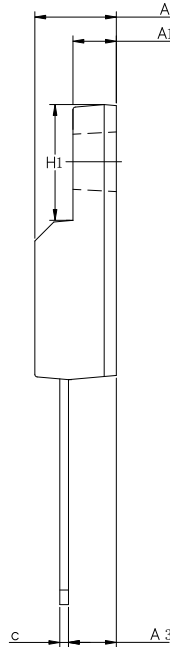
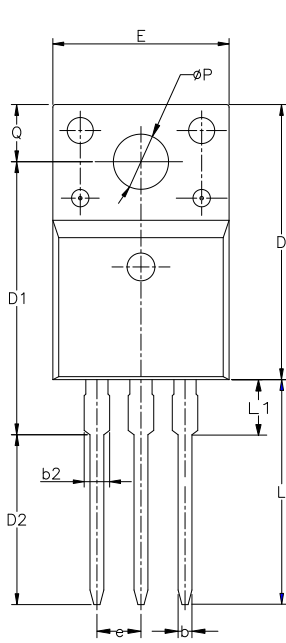
Unclamped Inductive Switching Test Circuit & Waveform



**PACKAGE OUTLINE**

**TO-220F-3L**

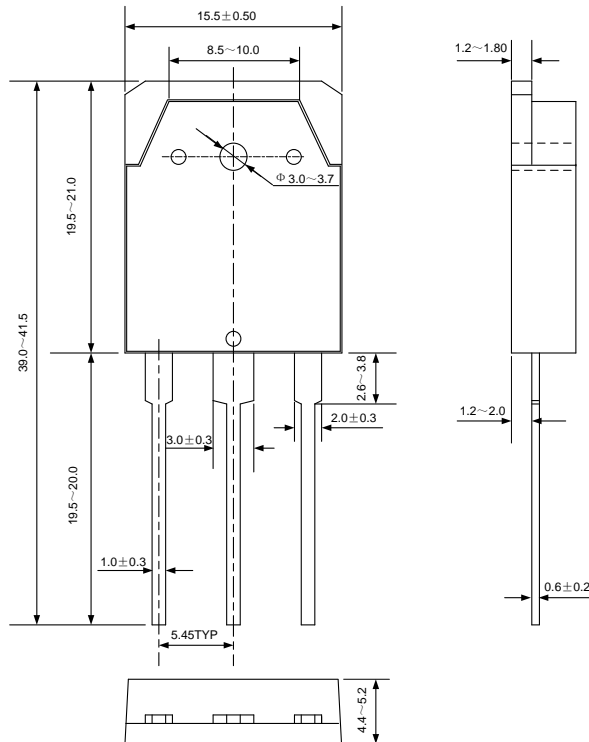
**UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
$\phi P$	3.00	3.18	3.40
Q	3.05	3.30	3.55

**TO-3P**

**UNIT: mm**



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Rev.:	1.6	Author:	Yin Zi
Revision History:			
1. Modify the EAS test condition.			

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Rev.:	1.5	Author:	Yin Zi
Revision History:			
1. Modify the package information of TO-220F-3L			

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Rev.:	1.4	Author:	Yin Zi
Revision History:			
1. Modify the thermal characteristics			

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Rev.:	1.3	Author:	Zhang Kefeng
Revision History:			
1. Modify the ordering information			

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Rev.:	1.2	Author:	Zhang Kefeng
Revision History:			
1. Change the schematic diagram of MOS			

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Rev.:	1.1	Author:	Zhang Kefeng
Revision History:			
1. Add the package of TO-3PN			

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Rev.:	1.0	Author:	Zhang Kefeng
Revision History:			
1. Initial release			

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