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Jameco Part Number 831859

# DAC0800/DAC0802

## 8-Bit Digital-to-Analog Converters

### General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 V<sub>p-p</sub> with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than  $\pm 1$  LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than  $\pm 0.1\%$  over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V<sub>LC</sub>, grounded. Changing the V<sub>LC</sub> potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full  $\pm 4.5$ V to  $\pm 18$ V power supply range; power dissipation is only 33 mW with  $\pm 5$ V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively.

### Features

- Fast settling output current: 100 ns
- Full scale error:  $\pm 1$  LSB
- Nonlinearity over temperature:  $\pm 0.1\%$
- Full scale current drift:  $\pm 10$  ppm/ $^{\circ}$ C
- High output compliance:  $-10$ V to  $+18$ V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range:  $\pm 4.5$ V to  $\pm 18$ V
- Low power consumption: 33 mW at  $\pm 5$ V
- Low cost

### Typical Applications

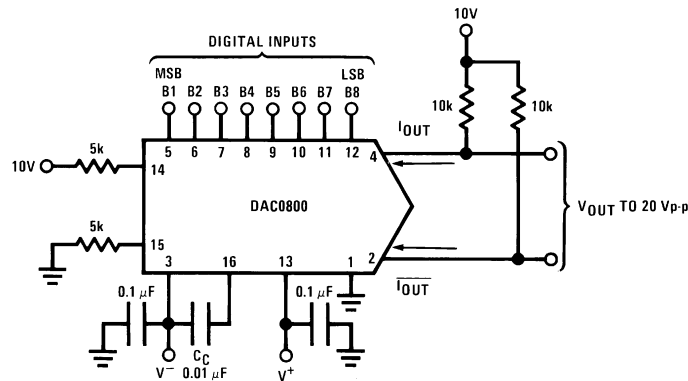


FIGURE 1.  $\pm 20$  V<sub>P-P</sub> Output Digital-to-Analog Converter (Note 5)

### Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A) (Note 1)		N Package (N16E) (Note 1)	SO Package (M16A)	
$\pm 0.1\%$ FS	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
$\pm 0.19\%$ FS	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	DAC0800LJ	DAC-08Q			
$\pm 0.19\%$ FS	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM

Note 1: Devices may be ordered by using either order number.

**Absolute Maximum Ratings** (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V^+ - V^-$ )	$\pm 18V$ or $36V$
Power Dissipation (Note 3)	500 mW
Reference Input Differential Voltage (V14 to V15)	$V^-$ to $V^+$
Reference Input Common-Mode Range (V14, V15)	$V^-$ to $V^+$
Reference Input Current	5 mA
Logic Inputs	$V^-$ to $V^-$ plus $36V$
Analog Current Outputs ( $V_{S-} = -15V$ )	4.25 mA
ESD Susceptibility (Note 4)	TBD V

Storage Temperature	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	$260^\circ\text{C}$
Dual-In-Line Package (ceramic)	$300^\circ\text{C}$
Surface Mount Package	
Vapor Phase (60 seconds)	$215^\circ\text{C}$
Infrared (15 seconds)	$220^\circ\text{C}$

**Operating Conditions** (Note 2)

	Min	Max	Units
Temperature ( $T_A$ )			
DAC0800L	-55	+125	$^\circ\text{C}$
DAC0800LC	0	+70	$^\circ\text{C}$
DAC0802LC	0	+70	$^\circ\text{C}$

**Electrical Characteristics**

The following specifications apply for  $V_S = \pm 15V$ ,  $I_{REF} = 2$  mA and  $T_{MIN} \leq T_A \leq T_{MAX}$  unless otherwise specified. Output characteristics refer to both  $I_{OUT}$  and  $I_{OUT-}$ .

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				$\pm 0.1$			$\pm 0.19$	%FS
$t_s$	Settling Time	To $\pm 1/2$ LSB, All Bits Switched "ON" or "OFF", $T_A = 25^\circ\text{C}$ DAC0800L DAC0800LC		100	135		100 100	135 150	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Each Bit All Bits Switched	$T_A = 25^\circ\text{C}$		35 35	60 60		35 35	60 60	ns
$TCI_{FS}$	Full Scale Tempco			$\pm 10$	$\pm 50$		$\pm 10$	$\pm 50$	ppm/ $^\circ\text{C}$
$V_{OC}$	Output Voltage Compliance	Full Scale Current Change < $1/2$ LSB, $R_{OUT} > 20$ M $\Omega$ Typ	-10		18	-10		18	V
$I_{FS4}$	Full Scale Current	$V_{REF} = 10.000V$ , $R_{14} = 5.000$ k $\Omega$ $R_{15} = 5.000$ k $\Omega$ , $T_A = 25^\circ\text{C}$	1.984	1.992	2.000	1.94	1.99	2.04	mA
$I_{FSS}$	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		$\pm 0.5$	$\pm 4.0$		$\pm 1$	$\pm 8.0$	$\mu\text{A}$
$I_{ZS}$	Zero Scale Current			0.1	1.0		0.2	2.0	$\mu\text{A}$
$I_{FSR}$	Output Current Range	$V^- = -5V$ $V^- = -8V$ to $-18V$	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA
$V_{IL}$ $V_{IH}$	Logic Input Levels Logic "0" Logic "1"	$V_{LC} = 0V$			0.8		2.0	0.8	V
$I_{IL}$ $I_{IH}$	Logic Input Current Logic "0" Logic "1"	$V_{LC} = 0V$ $-10V \leq V_{IN} \leq +0.8V$ $2V \leq V_{IN} \leq +18V$		-2.0 0.002	-10 10		-2.0 0.002	-10 10	$\mu\text{A}$
$V_{IS}$	Logic Input Swing	$V^- = -15V$	-10		18	-10		18	V
$V_{THR}$	Logic Threshold Range	$V_S = \pm 15V$	-10		13.5	-10		13.5	V
$I_{15}$	Reference Bias Current			-1.0	-3.0		-1.0	-3.0	$\mu\text{A}$
$dI/dt$	Reference Input Slew Rate	(Figure 11)	4.0	8.0		4.0	8.0		mA/ $\mu\text{s}$
$PSSI_{FS+}$ $PSSI_{FS-}$	Power Supply Sensitivity	$4.5V \leq V^+ \leq 18V$ $-4.5V \leq V^- \leq 18V$ $I_{REF} = 1\text{mA}$		0.0001	0.01		0.0001	0.01	%/%

## Electrical Characteristics (Continued)

The following specifications apply for  $V_S = \pm 15V$ ,  $I_{REF} = 2\text{ mA}$  and  $T_{MIN} \leq T_A \leq T_{MAX}$  unless otherwise specified. Output characteristics refer to both  $I_{OUT}$  and  $\overline{I_{OUT}}$ .

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
I+ I-	Power Supply Current	$V_S = \pm 5V$ , $I_{REF} = 1\text{ mA}$		2.3 -4.3	3.8 -5.8		2.3 -4.3	3.8 -5.8	mA mA
		$V_S = 5V$ , $-15V$ , $I_{REF} = 2\text{ mA}$		2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8	mA mA
I+ I-	Power Supply Current	$V_S = \pm 15V$ , $I_{REF} = 2\text{ mA}$		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8	mA mA
		Power Dissipation	$\pm 5V$ , $I_{REF} = 1\text{ mA}$	33	48		33	48	mW
P <sub>D</sub>	Power Dissipation	$5V$ , $-15V$ , $I_{REF} = 2\text{ mA}$	108	136		108	136	mW	
		$\pm 15V$ , $I_{REF} = 2\text{ mA}$	135	174		135	174	mW	

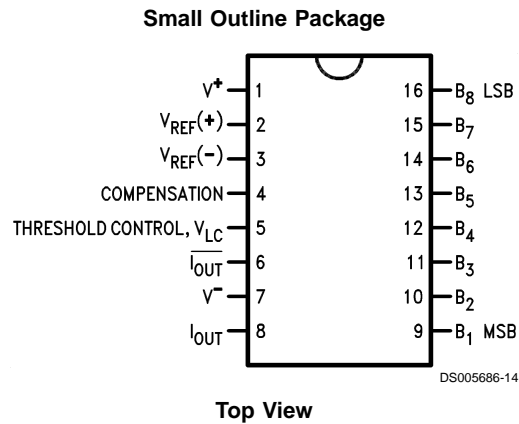
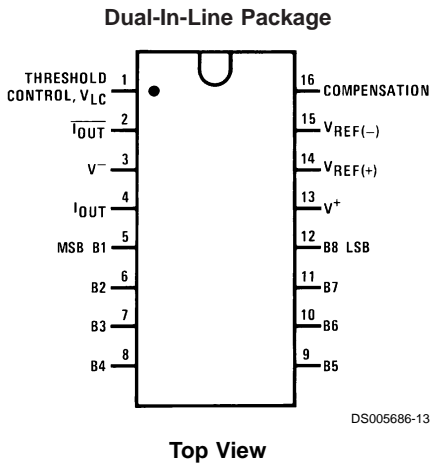
**Note 2:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 3:** The maximum junction temperature of the DAC0800 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the Dual-In-Line J package must be derated based on a thermal resistance of 100°C/W, junction-to-ambient, 175°C/W for the molded Dual-In-Line N package and 100°C/W for the Small Outline M package.

**Note 4:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.

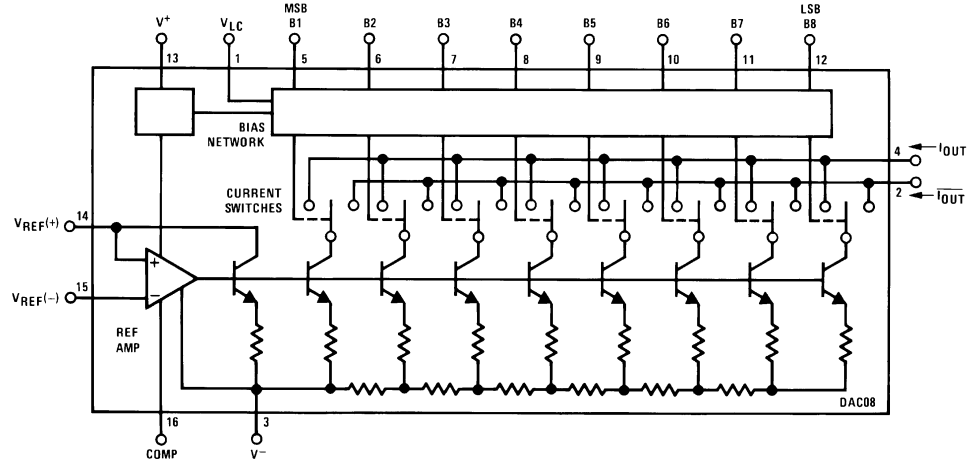
**Note 5:** Pin-out numbers for the DAC080X represent the Dual-In-Line package. The Small Outline package pin-out differs from the Dual-In-Line package.

## Connection Diagrams



See Ordering Information

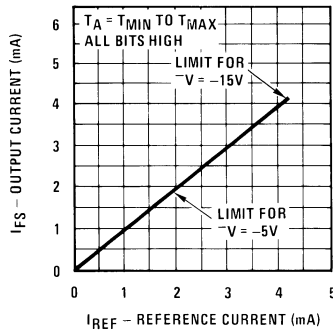
## Block Diagram (Note 5)



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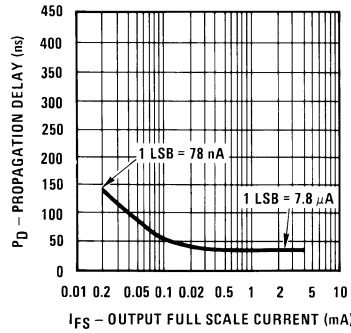
## Typical Performance Characteristics

### Full Scale Current vs Reference Current



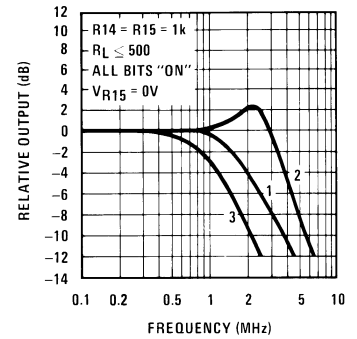
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### LSB Propagation Delay vs $I_{FS}$



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### Reference Input Frequency Response



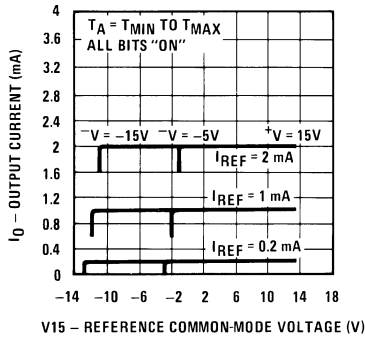
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Curve 1:  $C_C = 15 \text{ pF}$ ,  $V_{IN} = 2 \text{ Vp-p}$  centered at 1V.

Curve 2:  $C_C = 15 \text{ pF}$ ,  $V_{IN} = 50 \text{ mVp-p}$  centered at 200 mV.

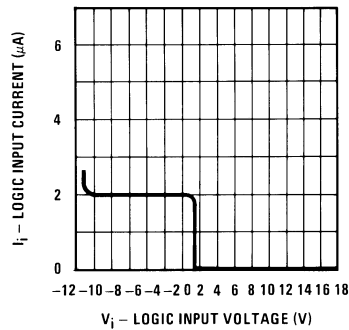
Curve 3:  $C_C = 0 \text{ pF}$ ,  $V_{IN} = 100 \text{ mVp-p}$  centered at 0V and applied through  $50\Omega$  connected to pin 14.2V applied to R14.

### Reference Amp Common-Mode Range



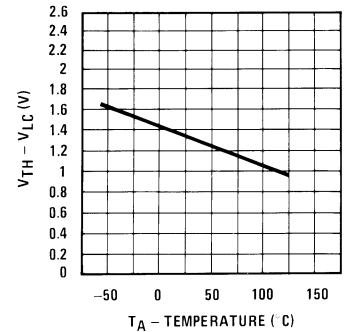
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### Logic Input Current vs Input Voltage



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### $V_{TH} - V_{LC}$ vs Temperature

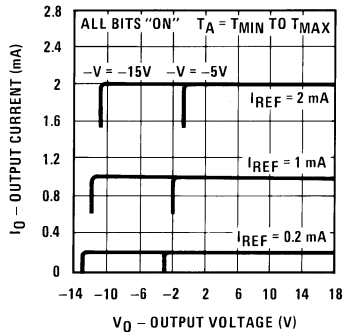


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Note. Positive common-mode range is always  $(V+) - 1.5V$ .

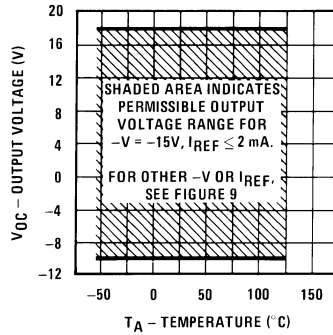
# Typical Performance Characteristics (Continued)

**Output Current vs Output Voltage (Output Voltage Compliance)**



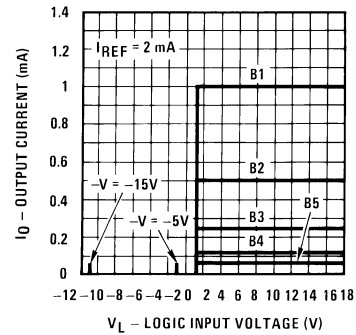
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**Output Voltage Compliance vs Temperature**



DS005686-29

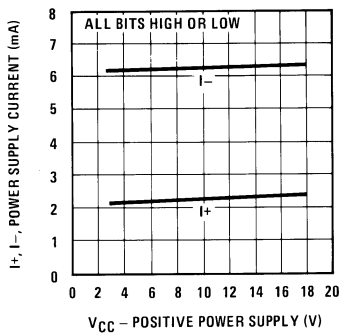
**Bit Transfer Characteristics**



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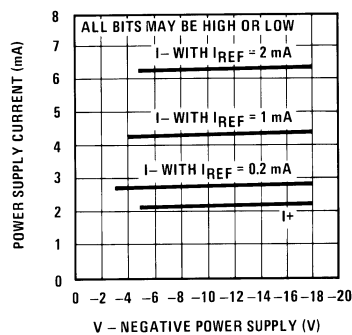
Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range ( $V_{LC} = 0V$ ).

**Power Supply Current vs +V**



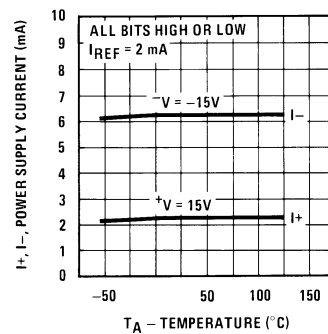
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**Power Supply Current vs -V**



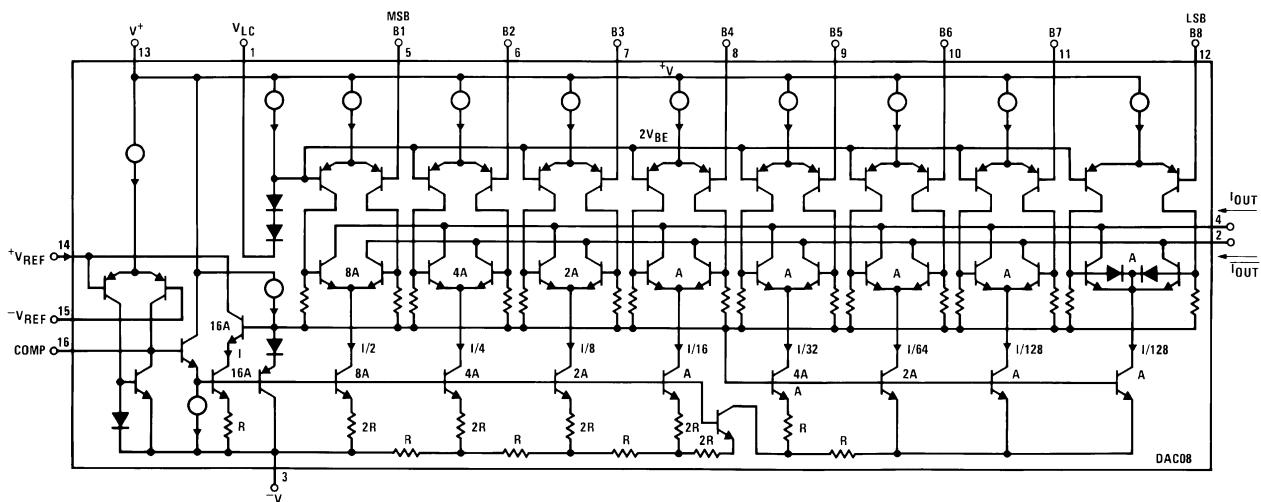
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**Power Supply Current vs Temperature**



DS005686-33

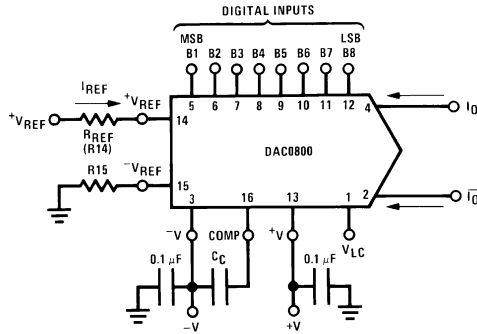
## Equivalent Circuit



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FIGURE 2.

# Typical Applications

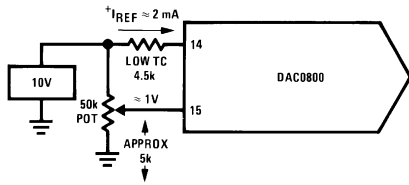


DS005686-5

$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

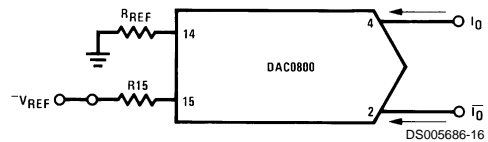
$I_O + \bar{I}_O = I_{FS}$  for all logic states  
 For fixed reference, TTL operation, typical values are:  
 $V_{REF} = 10.000V$   
 $R_{REF} = 5.000k$   
 $R15 = R_{REF}$   
 $C_C = 0.01 \mu F$   
 $V_{LC} = 0V$  (Ground)

FIGURE 3. Basic Positive Reference Operation (Note 5)



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FIGURE 4. Recommended Full Scale Adjustment Circuit (Note 5)

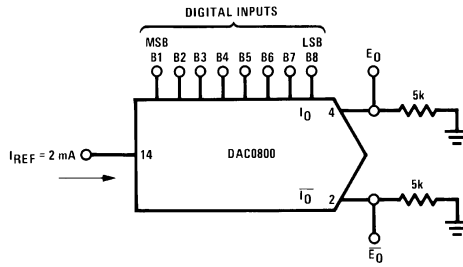


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$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note:  $R_{REF}$  sets  $I_{FS}$ ;  $R15$  is for bias current cancellation

FIGURE 5. Basic Negative Reference Operation (Note 5)

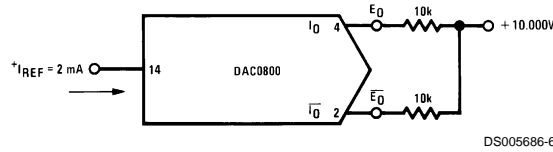


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	B1	B2	B3	B4	B5	B6	B7	B8	$I_O$ mA	$\bar{I}_O$ mA	$E_O$	$\bar{E}_O$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000
Full Scale-LSB	1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale-LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

FIGURE 6. Basic Unipolar Negative Operation (Note 5)

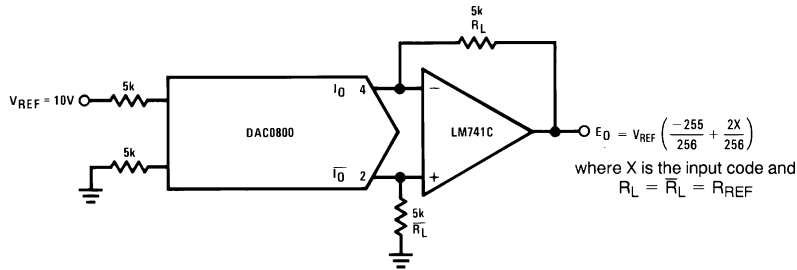
## Typical Applications (Continued)



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	B1	B2	B3	B4	B5	B6	B7	B8	$E_O$	$\bar{E}_O$
Pos. Full Scale	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos. Full Scale-LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale-LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920

FIGURE 7. Basic Bipolar Output Operation (Note 5)

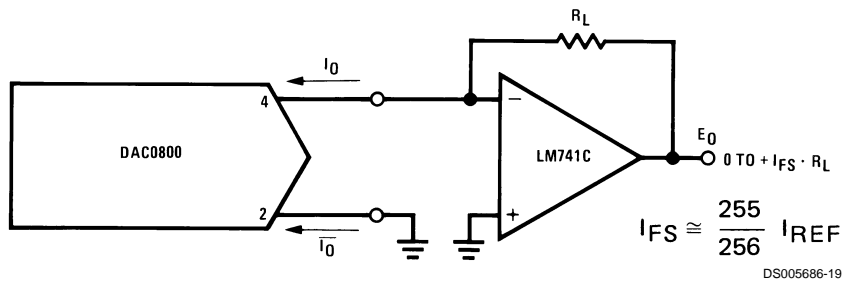


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If  $R_L = \bar{R}_L$  within  $\pm 0.05\%$ , output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	$E_O$
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale-LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(-)Zero Scale	0	1	1	1	1	1	1	1	-0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	-9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	-9.960

FIGURE 8. Symmetrical Offset Binary Operation (Note 5)



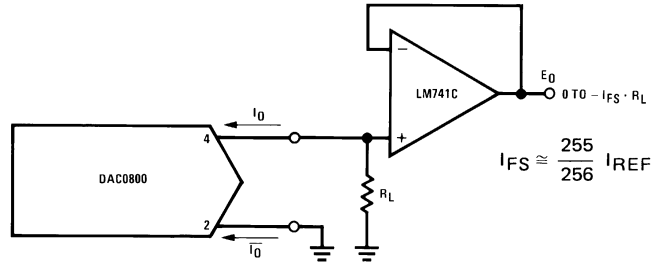
DS005686-19

For complementary output (operation as negative logic DAC), connect inverting input of op amp to  $\bar{I}_O$  (pin 2), connect  $I_O$  (pin 4) to ground.

FIGURE 9. Positive Low Impedance Output Operation (Note 5)



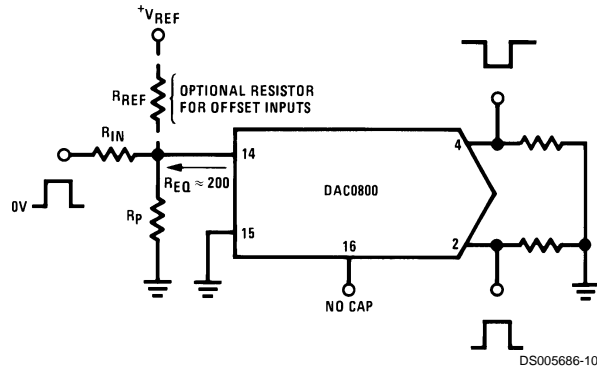
Typical Applications (Continued)



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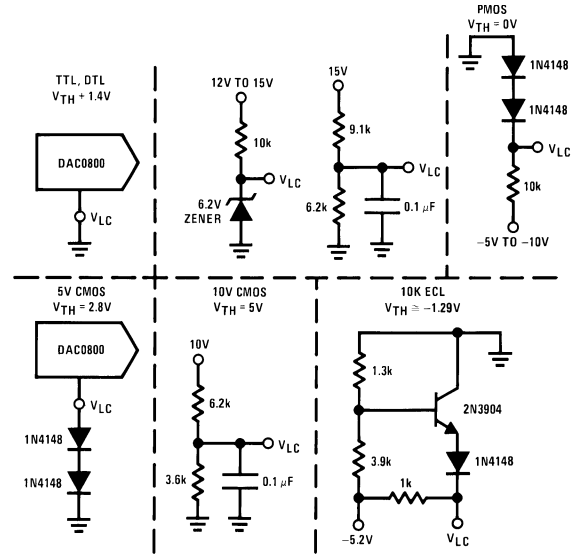
For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to  $\bar{I}_O$  (pin 2); connect  $I_O$  (pin 4) to ground.

FIGURE 10. Negative Low Impedance Output Operation (Note 5)



Typical values:  $R_{IN}=5k, +V_{IN}=10V$

FIGURE 11. Pulsed Reference Operation (Note 5)

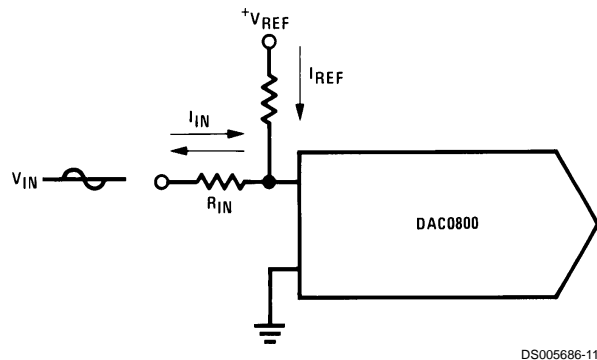


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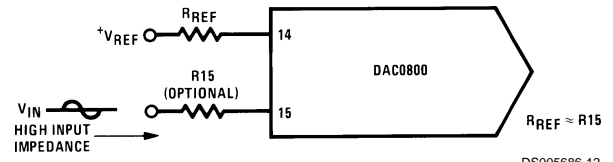
$V_{TH} = V_{LC} + 1.4V$   
 15V CMOS, HTL, HNIL  
 $V_{TH} = 7.6V$

Note. Do not exceed negative logic input range of DAC.

FIGURE 12. Interfacing with Various Logic Families



(a)  $I_{REF} \geq$  peak negative swing of  $I_{IN}$



(b)  $+V_{REF}$  must be above peak positive swing of  $V_{IN}$

FIGURE 13. Accommodating Bipolar References (Note 5)

Typical Applications (Continued)

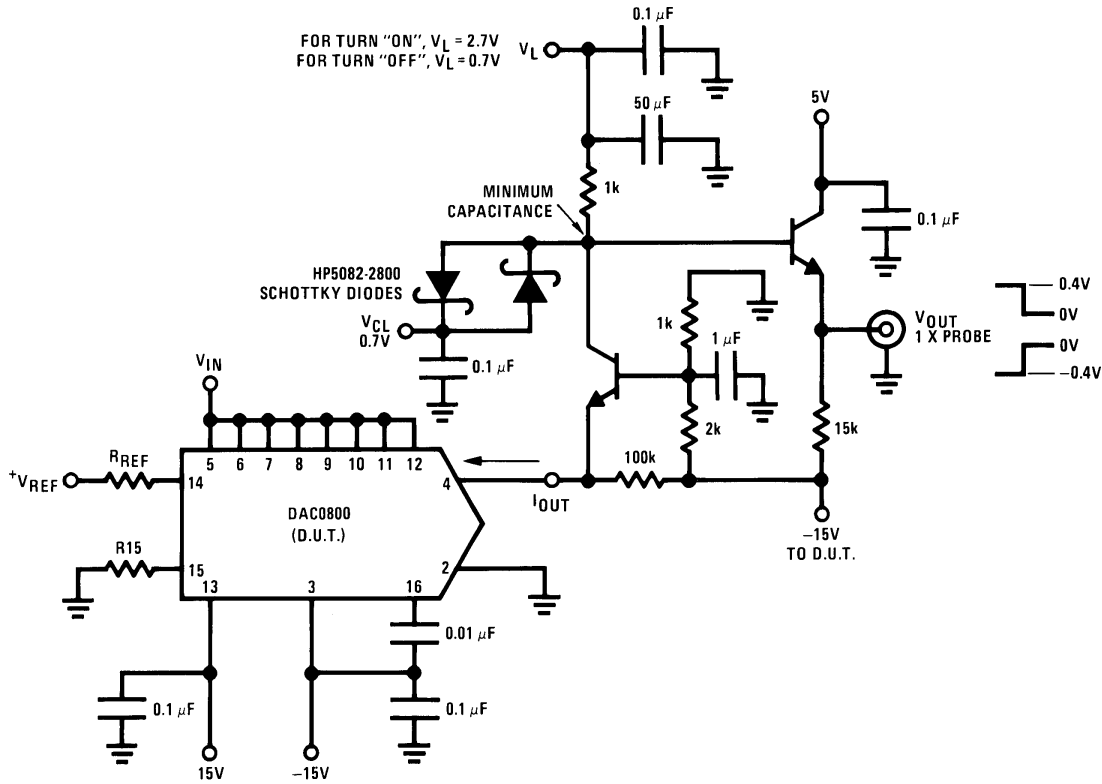
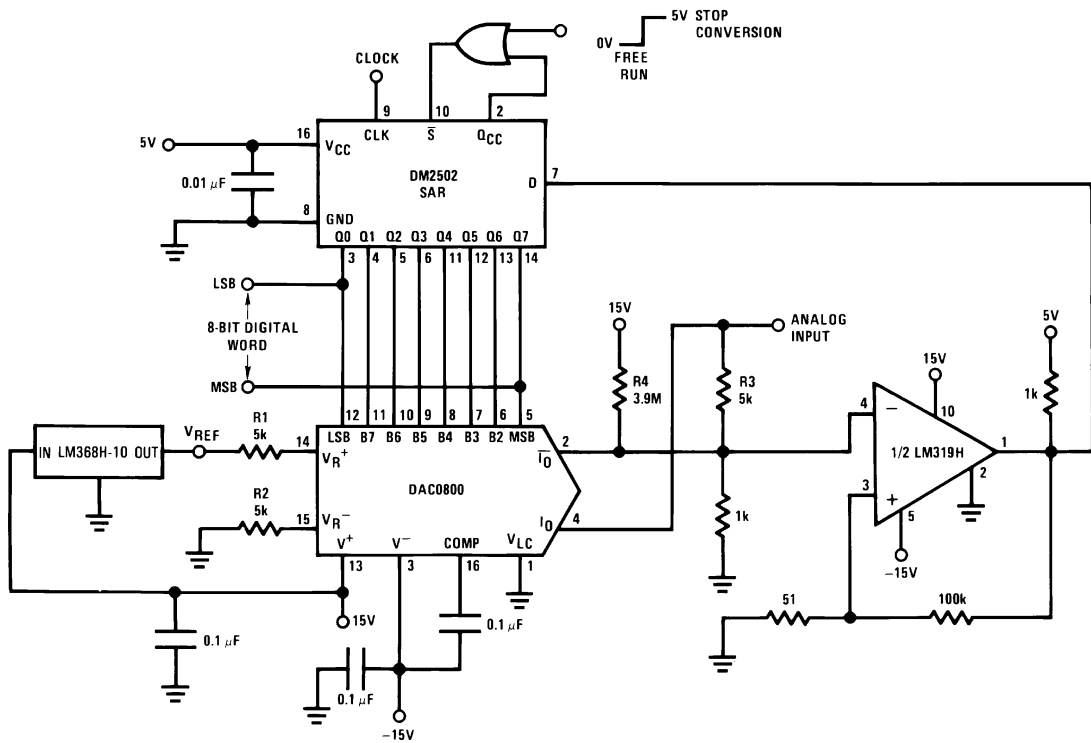


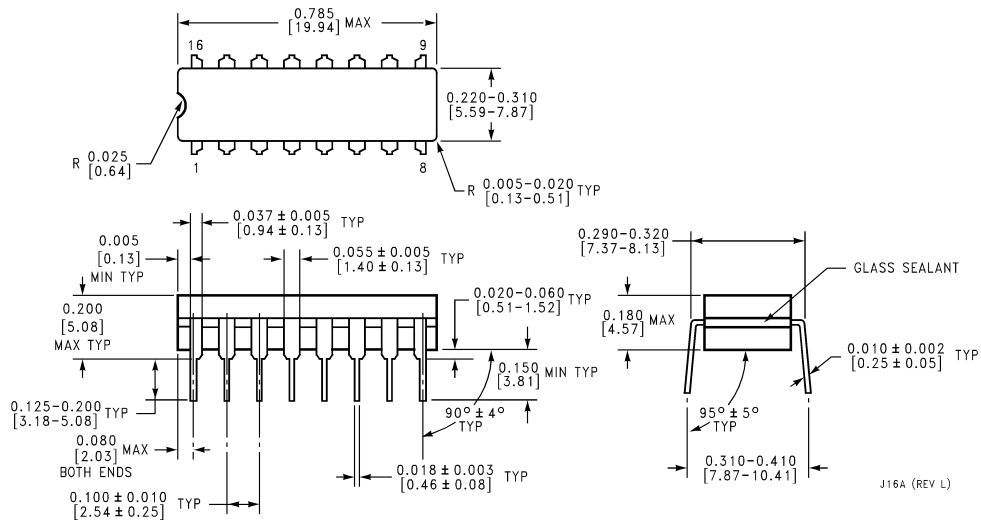
FIGURE 14. Settling Time Measurement (Note 5)



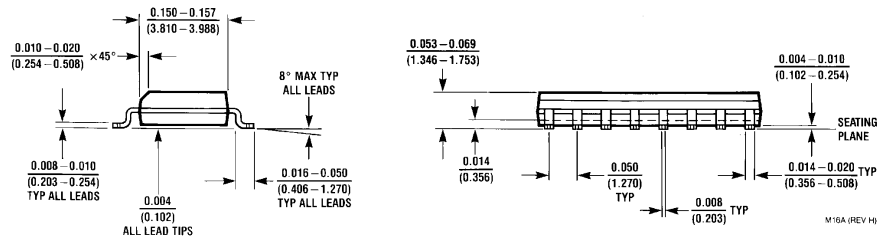
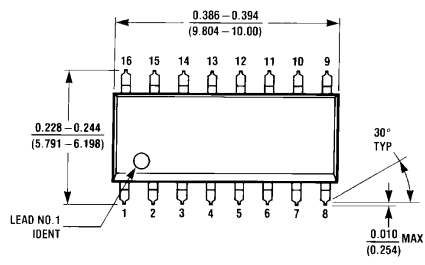
Note. For 1  $\mu s$  conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 k $\Omega$  and R4 to 2 M $\Omega$ .

FIGURE 15. A Complete 2  $\mu s$  Conversion Time, 8-Bit A/D Converter (Note 5)

**Physical Dimensions** inches (millimeters) unless otherwise noted

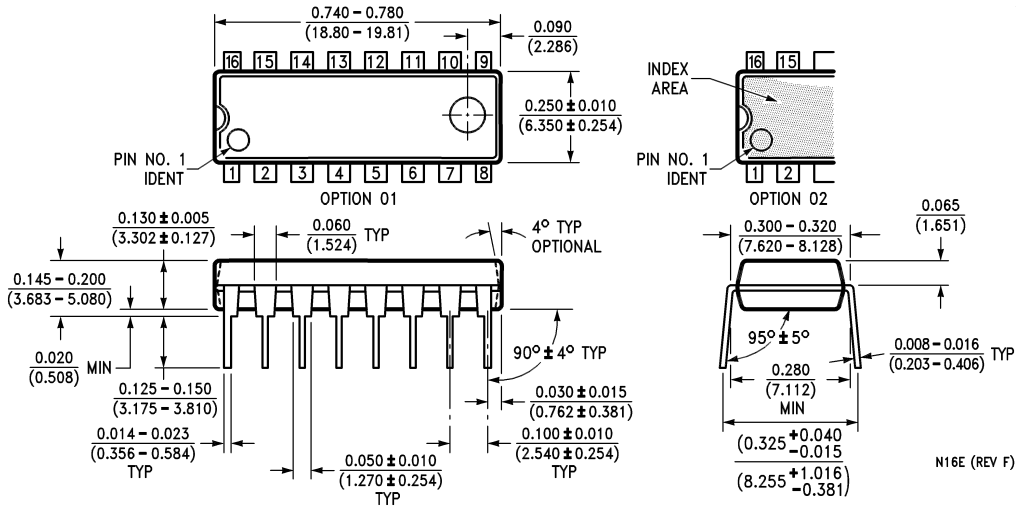


**Molded Small Outline Package (SO)**  
**Order Numbers DAC0800LCM,**  
**or DAC0802LCM**  
**NS Package Number M16A**



**Molded Small Outline Package (SO)**  
**Order Numbers DAC0800LCM,**  
**or DAC0802LCM**  
**NS Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**Molded Dual-In-Line Package**  
**Order Numbers DAC0800, DAC0802**  
**NS Package Number N16E**

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