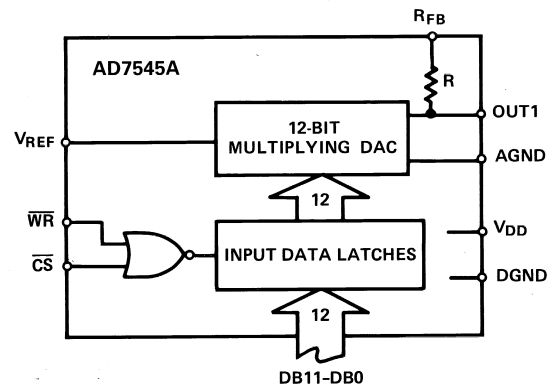


FEATURES

- Improved Version of AD7545
- Fast Interface Timing
- All Grades 12-Bit Accurate
- 20-Lead DIP and Surface Mount Packages
- Low Cost

FUNCTIONAL BLOCK DIAGRAM

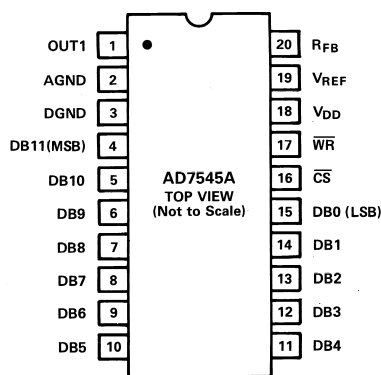


GENERAL DESCRIPTION

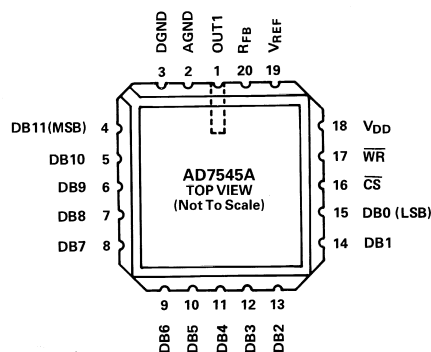
The AD7545A, a 12-bit CMOS multiplying DAC with internal data latches, is an improved version of the industry standard AD7545. This new design features a \overline{WR} pulse width of 100 ns, which allows interfacing to a much wider range of fast 8-bit and 16-bit microprocessors. It is loaded by a single 12-bit-wide word under the control of the \overline{CS} and \overline{WR} inputs; tying these control inputs low makes the input latches transparent, allowing unbuffered operation of the DAC.

PIN CONFIGURATIONS

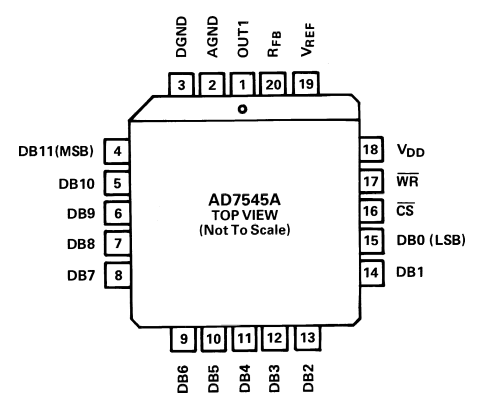
DIP/SOIC



LCCC



PLCC



REV. C

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AD7545A—SPECIFICATIONS ($V_{REF} = \pm 10\text{ V}$, $V_{OUT1} = 0\text{ V}$, $AGND = DGND$ unless otherwise noted)

Parameter	Version	$V_{DD} = +5\text{ V}$ Limits		$V_{DD} = +15\text{ V}$ Limits		Units	Test Conditions/Comments
		$T_A = +25^\circ\text{C}$	$T_{MIN}-T_{MAX}^1$	$T_A = +25^\circ\text{C}$	$T_{MIN}-T_{MAX}^1$		
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	Endpoint Measurement All Grades Guaranteed 12-Bit Monotonic Over Temperature Measured Using Internal R_{FB} . DAC Register Loaded with All 1s. $\Delta V_{DD} = \pm 5\%$ $DB0-DB11 = 0\text{ V}$; \overline{WR} , $\overline{CS} = 0\text{ V}$
Relative Accuracy	K, B, T	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	LSB max	
	L, C, U	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	LSB max	
Differential Nonlinearity	All	± 1	± 1	± 1	± 1	LSB max	
Gain Error	K, B, T	± 3	± 4	± 3	± 4	LSB max	
	L, C, U	± 1	± 2	± 1	± 2	LSB max	
Gain Temperature Coefficient ²	All	± 5	± 5	± 5	± 5	ppm/ $^\circ\text{C}$ max	
$\Delta\text{Gain}/\Delta\text{Temperature}$	All	± 2	± 2	± 2	± 2	ppm/ $^\circ\text{C}$ typ	
DC Supply Rejection ²	All	0.002	0.004	0.002	0.004	% per % max	
$\Delta\text{Gain}/\Delta V_{DD}$	All	0.002	0.004	0.002	0.004	% per % max	
Output Leakage Current at OUT1	K, L	10	50	10	50	nA max	
	B, C	10	50	10	50	nA max	
	T, U	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Current Settling Time ²	All	1	1	1	1	μs max	T_O 1/2 LSB. OUT1 Load = 100 Ω , $C_{EXT} = 13\text{ pF}$. DAC Output Measured from Falling Edge of \overline{WR} , $\overline{CS} = 0\text{ V}$.
Propagation Delay ² (from Digital Input Change to 90% of Final Analog Output)	All	200	–	150	–	ns max	OUT1 Load = 100 Ω , $C_{EXT} = 13\text{ pF}$ ³
Digital-to-Analog Glitch Impulse	All	5	–	5	–	nV sec typ	$V_{REF} = AGND$. OUT1 Load = 100 Ω , Alternately Loaded with All 0s and 1s.
AC Feedthrough ^{2, 4} At OUT1	All	5	5	5	5	mV p-p typ	$V_{REF} = \pm 10\text{ V}$, 10 kHz Sine Wave
REFERENCE INPUT							
Input Resistance (Pin 19 to GND)	All	10 20	10 20	10 20	10 20	k Ω min k Ω max	Input Resistance TC = –300 ppm/ $^\circ\text{C}$ typ Typical Input Resistance = 15 k Ω
ANALOG OUTPUTS							
Output Capacitance ²							
C_{OUT1}	All	70	70	70	70	pF max	$DB0-DB11 = 0\text{ V}$, \overline{WR} , $\overline{CS} = 0\text{ V}$
C_{OUT1}	All	150	150	150	150	pF max	$DB0-DB11 = 0\text{ V}$, \overline{WR} , $\overline{CS} = 0\text{ V}$
DIGITAL INPUTS							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	$V_{IN} = 0$ or V_{DD}
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current ⁵ I_{IN}	All	± 1	± 10	± 1	± 10	μA max	
Input Capacitance ² $DB0-DB11$, \overline{WR} , \overline{CS}	All	8	8	8	8	pF max	
	All	8	8	8	8	pF max	
SWITCHING CHARACTERISTICS²							
Chip Select to Write Setup Time t_{CS}	K, B, L, C T, U	100 100	130 170	75 75	85 95	ns min ns min	See Timing Diagram $t_{CS} \geq t_{WR}$, $T_{CH} \geq 0$
Chip Select to Write Hold Time t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width t_{WR}	K, B, L, C T, U	100 100	130 170	75 75	85 95	ns min ns min	
Data Setup Time t_{DS}	All	100	150	60	80	ns min	
Data Hold Time t_{DH}	All	5	5	5	5	ns min	
	All	5	5	5	5	ns min	
	All	5	5	5	5	ns min	
POWER SUPPLY							
V_{DD}	All	5	5	15	15	V	$\pm 5\%$ For Specified Performance
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	All	100	100	100	100	μA max	All Digital Inputs 0 V or V_{DD}
	All	10	10	10	10	μA typ	All Digital Inputs 0 V or V_{DD}

NOTES

¹Temperature range as follows: K, L Versions = 0 $^\circ\text{C}$ to +70 $^\circ\text{C}$; B, C Versions = –25 $^\circ\text{C}$ to +85 $^\circ\text{C}$; T, U Versions = –55 $^\circ\text{C}$ to +125 $^\circ\text{C}$.

²Sample tested to ensure compliance.

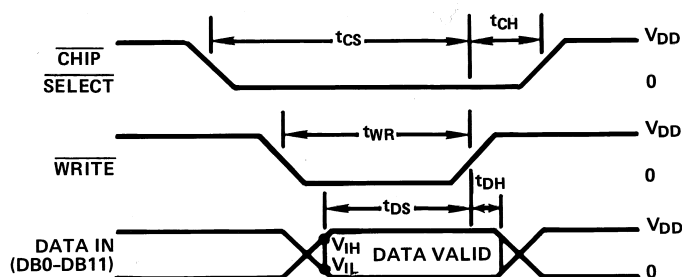
³ $DB0-DB11 = 0\text{ V}$ to V_{DD} or V_{DD} to 0 V.

⁴Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

⁵Logic inputs are MOS gates. Typical input current (+25 $^\circ\text{C}$) is less than 1 nA.

Specifications subject to change without notice.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:

\overline{CS} and \overline{WR} low, DAC responds to data bus (DB0-DB11) inputs.

HOLD MODE:

Either \overline{CS} or \overline{WR} high, data bus (DB0-DB11) is locked out; DAC holds last data present when \overline{WR} or \overline{CS} assumed high state.

NOTES:

$V_{DD} = +5V$; $t_r = t_f = 20ns$
 $V_{DD} = +15V$; $t_r = t_f = 40ns$
 All input signal rise and fall times measured from 10% to 90% of V_{DD} .
 Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

ABSOLUTE MAXIMUM RATINGS*

($T_A = +25^\circ C$ unless otherwise noted)

V_{DD} to DGND	-0.3 V, +17 V
Digital Input Voltage to DGND	-0.3 V, $V_{DD} + 0.3$ V
V_{RFB} , V_{REF} to DGND	± 25 V
V_{PIN1} to DGND	-0.3 V, $V_{DD} + 0.3$ V
AGND to DGND	-0.3 V, $V_{DD} + 0.3$ V
Power Dissipation (Any Package) to $75^\circ C$	450 mW
Derates above $75^\circ C$ by	6 mW/ $^\circ C$

Operating Temperature Range

Commercial (KN, LN, KP, LP) Grades	... 0 $^\circ C$ to +70 $^\circ C$
Industrial (BQ, CQ, BE, CE) Grades	... -25 $^\circ C$ to +85 $^\circ C$
Extended (TQ, UQ, TE, UE) Grades	... -55 $^\circ C$ to +125 $^\circ C$
Storage Temperature	... -65 $^\circ C$ to +150 $^\circ C$
Lead Temperature (Soldering, 10 secs)	... +300 $^\circ C$

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model ¹	Temperature Range	Relative Accuracy $T_{MIN}-T_{MAX}$	Gain Error $T_{MIN}-T_{MAX}$	Package Options ²
AD7545AKN	0 $^\circ C$ to +70 $^\circ C$	$\pm 1/2$	± 4	N-20
AD7545ALN	0 $^\circ C$ to +70 $^\circ C$	$\pm 1/2$	± 2	N-20
AD7545AKR	0 $^\circ C$ to +70 $^\circ C$	$\pm 1/2$	± 4	R-20
AD7545AKP	0 $^\circ C$ to +70 $^\circ C$	$\pm 1/2$	± 4	P-20A
AD7545ALP	0 $^\circ C$ to +70 $^\circ C$	$\pm 1/2$	± 2	P-20A
AD7545ABQ	-25 $^\circ C$ to +85 $^\circ C$	$\pm 1/2$	± 4	Q-20
AD7545ACQ	-25 $^\circ C$ to +85 $^\circ C$	$\pm 1/2$	± 2	Q-20
AD7545ABE	-25 $^\circ C$ to +85 $^\circ C$	$\pm 1/2$	± 4	E-20A
AD7545ACE	-25 $^\circ C$ to +85 $^\circ C$	$\pm 1/2$	± 2	E-20A
AD7545ATQ	-55 $^\circ C$ to +125 $^\circ C$	$\pm 1/2$	± 4	Q-20
AD7545AUQ	-55 $^\circ C$ to +125 $^\circ C$	$\pm 1/2$	± 2	Q-20
AD7545ATE	-55 $^\circ C$ to +125 $^\circ C$	$\pm 1/2$	± 4	E-20A
AD7545AUE	-55 $^\circ C$ to +125 $^\circ C$	$\pm 1/2$	± 2	E-20A

NOTES

- ¹To order MIL-STD-883, Class B process parts, add /883B to part number. Contact local sales office for military data sheet.
- ²E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = CerDip; R = Small Outline IC.

AD7545A

CIRCUIT INFORMATION—D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A converter section of the AD7545A, and Figure 2 gives an approximate equivalent circuit. Note that the ladder termination resistor is connected to AGND. R is typically 15 kΩ.

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

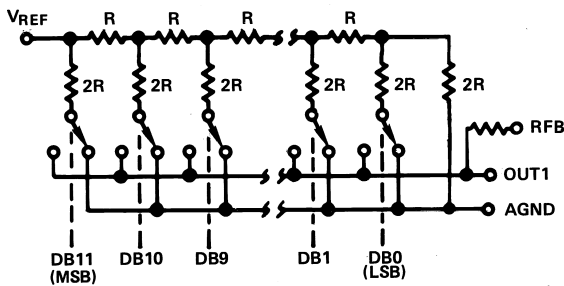


Figure 1. Simplified D/A Circuit of AD7545A

The capacitance at the OUT1 bus line, C_{OUT1} , is code-dependent and varies from 70 pF (all switches to AGND) to 150 pF (all switches to OUT1).

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R. Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

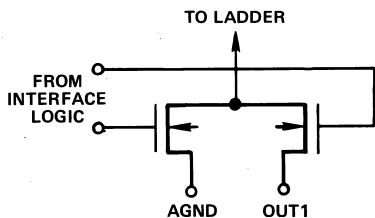


Figure 2. N-Channel Current Steering Switch

CIRCUIT INFORMATION—DIGITAL SECTION

Figure 3 shows the digital structure for one bit.

The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{\text{CS}}$ and $\overline{\text{WR}}$.

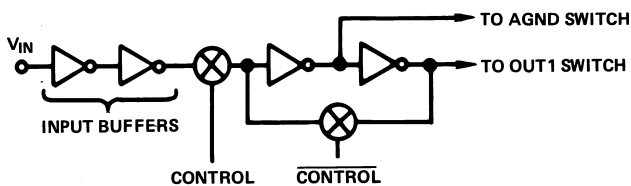


Figure 3. Digital Input Structure

The input buffers are simple CMOS inverters designed such that when the AD7545A is operated with $V_{DD} = 5$ V, the buffers convert TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts, the

input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545A may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With $V_{DD} = +15$ V the input logic levels are CMOS compatible only, i.e., 1.5 V and 13.5 V.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the AD7545A. Resistor R1 is used to trim for full scale. The L, C, U grades have a guaranteed maximum gain error of ± 1 LSB at $+25^\circ\text{C}$, and in many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that all the circuits of Figures 4, 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD} . Table II shows the code relationship for the circuit of Figure 4.

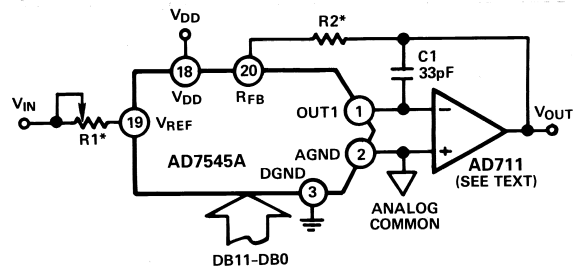


Figure 4. Unipolar Binary Operation

Table I. Recommended Trim Resistor Values vs. Grades

Trim Resistor	K/B/T	L/C/U
R1	200 Ω	100 Ω
R2	68 Ω	33 Ω

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Binary Number in DAC Register	Analog Output
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN} \left(\frac{4095}{4096} \right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN} \left(\frac{2048}{4096} \right) = -1/2 V_{IN}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{IN} \left(\frac{1}{4096} \right)$
0 0 0 0 0 0 0 0 0 0 0 0	0 Volts

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U₁ on the MSB line converts two's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive-OR instruction and the inverter omitted. R₃, R₄ and R₅ must be selected to match within 0.01%, and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R₃ value to R₄ causes both offset and full-scale error. Mismatch of R₅ to R₄ and R₃ causes full-scale error.

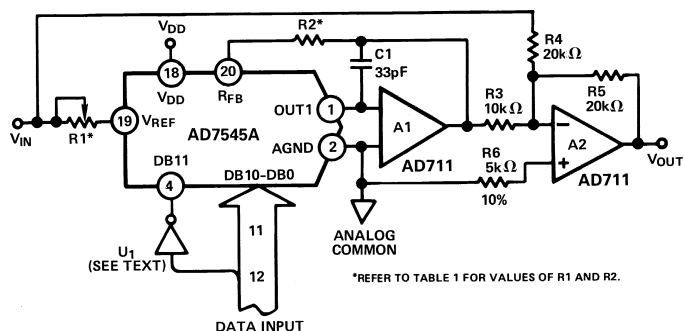


Figure 5. Bipolar Operation (Twos Complement Code)

Table III. Twos Complement Code Table for Circuit of Figure 5

Data Input	Analog Output
0 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN} \times \left(\frac{2047}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$+V_{IN} \times \left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0 Volts
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN} \times \left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN} \times \left(\frac{2048}{2048}\right)$

Figure 6 and Table IV show an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R₄ and R₅ should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R₄ and R₅ introduces a gain error. Refer to Reference 1 (supplemental application material) for additional information on these circuits.

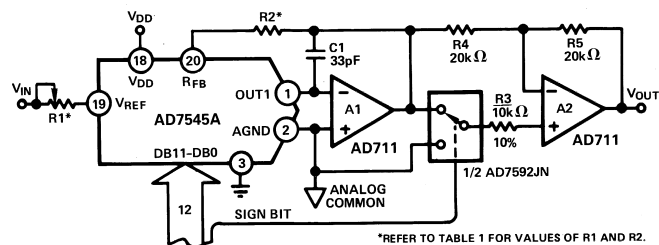


Figure 6. 12-Bit Plus Sign Magnitude Converter

Table IV. 12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 6

Sign Bit	Binary Numbers in DAC Register	Analog Output
0	1 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN} \times \left(\frac{4095}{4096}\right)$
0	0 0 0 0 0 0 0 0 0 0 0 0	0 Volts
1	0 0 0 0 0 0 0 0 0 0 0 0	0 Volts
1	1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN} \times \left(\frac{4095}{4096}\right)$

Note: Sign bit of "0" connects R₃ to GND.

APPLICATIONS HINTS

Output Offset: CMOS D/A converters such as Figures 4, 5 and 6 exhibit a code dependent output resistance which, in turn, can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified accuracy with V_{REF} at 10 V, it is recommended that V_{OS} be no greater than 0.25 mV, or (25 × 10⁻⁶) (V_{REF}), over the temperature range of operation. Suitable op amps are AD517 and AD711. The AD517 is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (150 μV max for lowest grade) and in most applications will not require an offset trim. The AD711 has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD711 may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545A. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545A AGND and DGND pins (1N914 or equivalent).

AD7545A

Invalid Data: When \overline{WR} and \overline{CS} are both low, the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which \overline{WR} is low, and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted signals or glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse, \overline{WR} , so it only occurs when data is valid.

Digital Glitches: Digital glitches result due to capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by screening the analog pins of the AD7545A (Pins 1, 2, 19, 20) from the digital pins by a ground track run between Pins 2 and 3 and between Pins 18 and 19 of the AD7545A.

Note how the analog pins are at one end (DIP) or side (LCC and PLCC) of the package and separated from the digital pins by V_{DD} and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital-to-analog sections of the AD7545A, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using $V_{DD} = +5$ volts. However, great care should be taken to ensure that the +5 V used to power the AD7545A is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545A has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 (such as in Figure 4) are used to adjust full-scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient to CMOS Multiplying DACs," Publication Number E630c-5-3/86.

SINGLE SUPPLY OPERATION

The ladder termination resistor of the AD7545A (Figure 1) is connected to AGND. This arrangement is particularly suitable for single supply operation because OUT1 and AGND may be biased at any voltage between DGND and V_{DD} . OUT1 and AGND should never go more than 0.3 volts less than DGND or an internal diode will be turned on and a heavy current may flow that will damage the device. (The AD7545A is, however, protected from the SCR latchup phenomenon prevalent in many CMOS devices.)

Figure 7 shows the AD7545A connected in a voltage switching mode. OUT1 is connected to the reference voltage and AGND is connected to DGND. The D/A converter output voltage is available at the V_{REF} pin and has a constant output impedance equal to R. R_{FB} is not used in this circuit and should be tied to OUT1 to minimize stray capacitance effects.

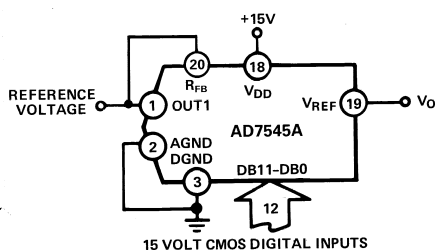


Figure 7. Single Supply Operation Using Voltage Switching Mode

The loading on the reference voltage source is code-dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions. To maintain linearity, the voltages at OUT1 and AGND should remain within 2.5 volts of each other, for a V_{DD} of 15 volts. If V_{DD} is reduced from 15 V, or the differential voltage between OUT1 and AGND is increased to more than 2.5 V, the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded. Figures 8 and 9 show typical curves illustrating this effect for various values of reference voltage and V_{DD} . If the output voltage is required to be offset from ground by some value, then OUT1 and AGND may be biased up. The effect on linearity and differential nonlinearity will be the same as reducing V_{DD} by the amount of the offset.

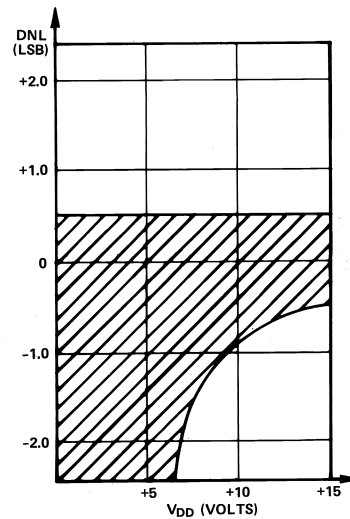


Figure 8. Differential Nonlinearity vs. V_{DD} for Figure 7 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for all Grades.

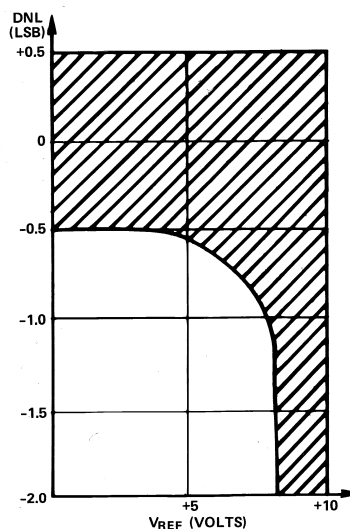
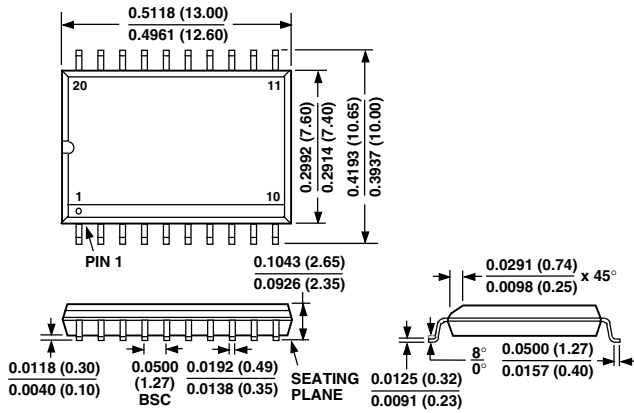


Figure 9. Differential Nonlinearity vs. Reference Voltage for Figure 7 Circuit. $V_{DD} = 15$ Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for all Grades.

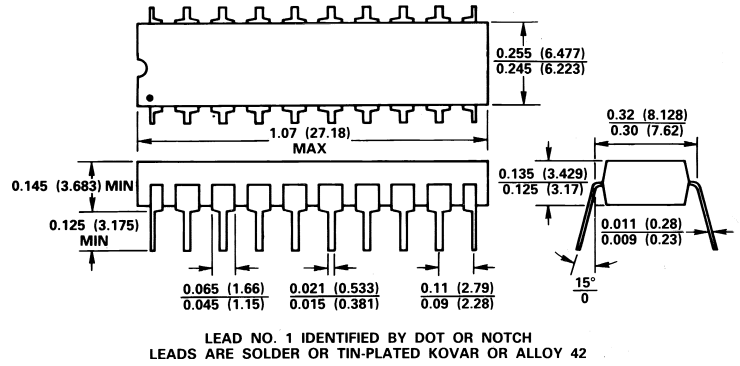
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

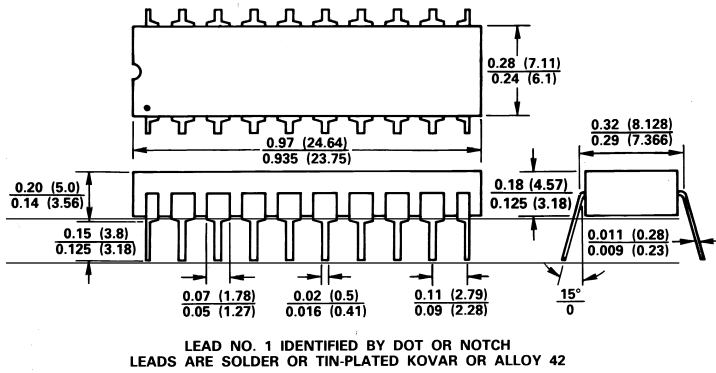
20-Lead SOIC (R-20)



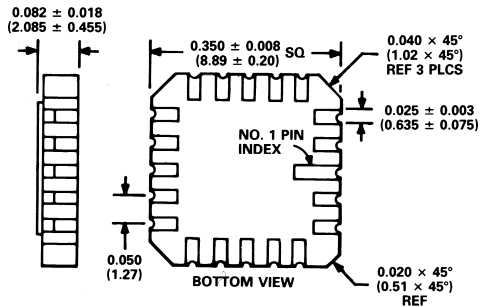
20-Lead Plastic DIP (N-20)



20-Lead Cerdip (Q-20)



20-Terminal Leadless Ceramic Chip Carrier (E-20A)



20-Terminal Plastic Leadless Chip Carrier (P-20A)

